CHARGE PUMP AND VOLTAGE DOUBLER USING THE SAME

CROSS-REFERENCE TO RELATED APPLICATION

This application claims the priority benefit of Taiwan application serial no. 91135002, filed December 3, 2002.

BACKGROUND OF THE INVENTION

Field of Invention

[0001] The present invention relates to a charge pump and a voltage doubler using the same. More particularly, the present invention relates to a charge pump comprising low-pressure fabricated metal-oxide-semiconductor (MOS) devices and a voltage double using the same.

Description of Related Art

[0002] Fig. 1A is a circuit diagram of a conventional charge pump. As shown in Fig. 1A, the charge pump 10 comprises two N-type metal oxide semiconductor (NMOS) transistors 102 and 104 and two capacitors 112 and 114. One source/drain terminal of the NMOS transistor 102 is electrically coupled to an input voltage V_{IN} terminal while the other source/drain terminal of the NMOS transistor 102 is electrically coupled to one terminal 112a of the capacitor 112. The substrate terminal of the NMOS transistor 102 is connected to ground and the gate terminal of the NMOS transistor 102 is connected to one terminal 114a of the capacitor 114. Voltage at the capacitor terminal 114a serves as an output voltage V_{01} of the charge pump 10. Similarly, one source/drain terminal of the

NMOS transistor 104 is electrically coupled to the input voltage V_{IN} terminal while the other source/drain terminal of the NMOS transistor 104 is electrically coupled to the capacitor terminal 114a. The substrate terminal of the NMOS transistor 104 is connected to ground and the gate terminal of the NMOS transistor 104 is electrically connected to the capacitor terminal 112a. Voltage at the capacitor terminal 112a serves as another output voltage V_{02} of the charge pump 10. In addition, the other terminal 112b of the capacitor 112 receives a clocking signal CK and the other terminal 114b of the capacitor 114 receives an inverse clocking signal CK' during operation.

[0003] Initially, voltage difference at the two terminals of both capacitors 112 and 114 is at 0V. Assume that the clocking signal CK is a signal having a voltage between 0 to V_1 during operation, the voltage V_1 is identical or greater than V_{IN} and the clocking signal CK is at a high potential level initially. At the beginning of operation, voltage difference between the ends of the capacitor 112 is maintained at 0V due to the capacitor property. Hence, voltage at the capacitor terminal 112a is raised to V_1. Under this condition, because the inverted clocking signal CK' is at 0V, the charge pump 10 outputs a voltage V_{01} of 0V and a voltage V_{02} of V_1. Thereafter, since $V_1 \geq V_{IN}$, the NMOS transistor 104 conducts and hence V_{IN} gradually charges up the capacitor 114. Consequently, after the passage of some time, voltage at the capacitor terminal 114a is raised to a level almost identical to V_{IN}.

[0004] When phase of the clocking signal CK reverses back to 0V (that is, phase of the inverted clocking signal CK' reverses back to V_1), voltage difference between the terminals 112a and 112b of the capacitor 112 is maintained during a transient period. Consequently, the capacitor terminal 112a returns to 0V. Similarly, because the voltage difference between the terminals 114a and 114b of the capacitor 114 is maintained during

a transient period when phase of the inverted clocking signal CK' reverses, voltage at the capacitor terminal 114a is pushed up to $V_{IN} + V_1$. In other words, during the transient phase inversion of the clocking signal CK, the output voltage V_{01} is $V_{IN} + V_1$ and the output voltage V_{02} is at 0V. Under this condition, the NMOS 104 is cut off and the NMOS transistor 102 conducts because the gate voltage (equivalent to the output voltage V_{01}) is greater than the input voltage V_{IN}. Thus, voltage at the capacitor terminal 112a gradually rises from 0V towards V_{IN}.

[0005] For the same reason, during the transient period when the phase of the clocking signal CK reverses, the output voltage V_{01} drops back to V_{IN} while the output voltage V_{02} rises up towards $V_{IN} + V_1$. In subsequent operations, the output voltages V_{01} and V_{02} will fluctuate in cycles between V_{IN} and $V_{IN} + V_1$.

[0006] However, for this type of circuit, the biggest voltage difference sustainable by the gate-substrate of the NMOS transistors 102 and 104 is $V_{IN} + V_1$. Therefore, the NMOS transistors 102 and 104 must be able to withstand a voltage greater than $V_{IN} + V_1$. In other words, the gate-substrate interface of the NMOS transistors 102 and 104 must be able to withstand a voltage difference equivalent to the output voltage value.

[0007] A voltage doubler that uses this type of charge pump was first disclosed in the article 'A High-Efficiency CMOS Voltage Doubler' of the IEEE Journal of Solid State Circuits, Vol. 33, No. 3, March 1998 by Philippe Deval and Mechel J. Declercq. Fig. 1B is a circuit diagram of the voltage doubler that uses the conventional charge pump design shown in Fig. 1A. The clocking signal CK varies cyclically between V_{IN} and 0V during operation. Hence, the output voltage V_{OUT} approaches $2*V_{IN}$. Similarly, the

gate-substrate interface of the NMOS transistors 122 and 124 must be able to sustain a voltage difference of at least $2*V_{IN}$.

SUMMARY OF THE INVENTION

[0008] Accordingly, one object of the present invention is to provide a charge pump and a voltage doubler using the same. Through the serial connection of a P-type metal oxide semiconductor (PMOS) transistor with an N-type metal oxide semiconductor (NMOS) transistor, metal oxide semiconductor (MOS) devices within the charge pump are subjected to a lower voltage differential at the gate-source, gate-substrate and gate-drain interface. Nevertheless, the same degree of voltage push-up as in the conventional technique is provided.

[0009] To achieve these and other advantages and in accordance with the purpose of the invention, as embodied and broadly described herein, the invention provides a charge pump. The charge pump has a voltage source, a signal source, a first and a second control signal generation unit, a first and a second output voltage generation unit and a first and a second capacitor. The voltage source provides an input voltage and the signal source provides a clocking signal and an inverted clocking signal for operation.

[0010] The first control signal generation unit receives an input voltage, the inverted clocking signal and a ground voltage and outputs a set of first control signals whose voltage levels are determined by the inverted clocking signal. The second control signal generation unit receives an input voltage, the clocking signal and a ground voltage and outputs a set of second control signals whose voltage levels are determined by the clocking signal.

[0011] The first output voltage generation unit has a first output terminal. The first output voltage generation unit receives the input voltage and the first control signal and determines if the circuit between the input voltage and the first output terminal becomes electrically conductive according to the first control signal. Similarly, the second output voltage generation unit has a second output terminal. The second output voltage generation unit receives the input voltage and the second control signal and determines if the circuit between the input voltage and the second output terminal becomes electrically conductive according to the second control signal.

[0012] A first capacitor terminal of the first capacitor receives the clocking signal. The other capacitor terminal of the first capacitor outputs the first output voltage and the capacitor terminal couples electrically with the first output terminal. A first capacitor terminal of the second capacitor receives the inverted clocking signal. The other capacitor terminal of the second capacitor outputs the second output voltage and the capacitor terminal couples electrically with the second output terminal.

[0013] In brief, voltage differential at the gate-substrate, gate-drain and gate source interface of various MOS devices inside the charge pump of this invention is smaller than the voltage differential at the same interfaces inside the MOS devices of a conventional charge pump. Hence, a low pressure CMOS fabrication process can be used to fabricate MOS devices having a voltage push-up capacity identical to the conventional technique but with a longer working life.

[0014] It is to be understood that both the foregoing general description and the following detailed description are exemplary, and are intended to provide further explanation of the invention as claimed.

BRIEF DESCRIPTION OF THE DRAWINGS

[0015] The accompanying drawings are included to provide a further understanding of the invention, and are incorporated in and constitute a part of this specification. The drawings illustrate embodiments of the invention and, together with the description, serve to explain the principles of the invention.

[0016] Fig. 1A is a circuit diagram of a conventional charge pump.

[0017] Fig. 1B is a circuit diagram of the voltage doubler that uses the conventional charge pump design shown in Fig. 1A.

[0018] Fig. 2 is a block diagram showing the circuit of a charge pump according to one preferred embodiment of this invention.

[0019] Fig. 3 is a block diagram showing the circuit of a voltage doubler according to one preferred embodiment of this invention.

[0020] Fig. 4 is an actual circuit diagram of a charge pump according to another preferred embodiment of this invention.

[0021] Fig. 5 is an actual circuit diagram of a voltage doubler according to another preferred embodiment of this invention.

DESCRIPTION OF THE PREFERRED EMBODIMENTS

[0022] Reference will now be made in detail to the present preferred embodiments of the invention, examples of which are illustrated in the accompanying drawings. Wherever possible, the same reference numbers are used in the drawings and the description to refer to the same or like parts.

[0023] Fig. 2 is a block diagram showing the circuit of a charge pump according to one preferred embodiment of this invention. As shown in Fig. 2, the charge pump

includes two control signal generation units 202 and 204, two output voltage generation units 206 and 208 and two capacitors 230 and 232. The control signal generation unit 202 receives an input voltage V_{IN} from a voltage source (not shown), a ground voltage and an inverted clocking signal CK' from a signal source (not shown), and generates a first control signal. The control signal generation unit 204 receives the input voltage V_{IN}, a ground voltage and a clocking signal CK from a signal source (not shown), and generates a second control signal. The clocking signal CK and the inverted clocking signal CK' have a phase inversion relationship.

[0024] In this embodiment, voltage level of the first control signal from the control signal generation unit 202 is determined by the inverted clocking signal CK'. In other words, the inverted clocking signal CK' at a low potential may prompt the control signal generation unit 202 to produce a high or a low first control signal according to the circuit design. Conversely, the inverted clocking signal CK' at a high potential may also prompt the control signal generation unit 202 to produce a high or a low first control signal. In a similar way, the relationship between the control signal generation unit 204 and the second control signal closely matches the relationship between the control signal generation unit 202 and the first control signal.

[0025] The output voltage generation unit 206 receives the voltage VIN and the first control signal and outputs via an output terminal 220. The output voltage generation unit 208 receives the voltage V_{IN} and the second control signal and outputs via an output terminal 222. For the output voltage generation unit 206, whether the input voltage V_{IN} is connected to the first output terminal 220 by an internal circuit depends on the voltage level of the first control signal. For example, if the first control signal is at a high potential, the circuit between the input voltage V_{IN} and the first output terminal 220 is

connected. On the other hand, if the first control signal is at a low potential, circuit connection between the input voltage V_{IN} and the first output terminal 220 is cut. Similarly, for the output voltage generation unit 208, if the second control signal is at a high potential, the circuit between the input voltage V_{IN} and the second output terminal 222 is connected. On the contrary, if the second control signal is at a low potential, circuit connection between the input voltage V_{IN} and the second output terminal 222 is cut. Obviously, contrary or different response to the control signal for the output voltage generation units 206 and 208 is also possible.

[0026] The charge pump circuit in Fig. 2 further includes two capacitors 230 and 232. One end of the capacitor 230 receives the clocking signal CK while the other end of the capacitor 230 couples electrically to the first output terminal 220. Meanwhile, the first output voltage is output from the output terminal V_{OUT1}. Similarly, one end of the capacitor 232 receives the inverted clocking signal CK' while the other end of the capacitor 232 couples electrically with the second output terminal 222. The second output voltage is output from the output terminal V_{OUT2}.

[0027] Fig. 3 is a block diagram showing the circuit of a voltage doubler according to one preferred embodiment of this invention. In Fig. 3, the charge pump structure and operating method is similar the one shown in Fig. 2 and hence detailed description is omitted. In general, the largest voltage from the output terminals V_{OUT1} and V_{OUT2} is roughly twice that of the input voltage V_{IN}. Hence, voltage doubling is obtained if the output voltage switching unit 340 picks up the one having the highest voltage to be the output voltage at the output terminal V_0 among the output terminals V_{OUT1} and V_{OUT2}.

[0028] In the following, circuit elements inside a charge pump and an output voltage switching unit are further disclosed. Note that the circuit elements and structure

in the subsequent embodiment is just one among many possible arrangements and hence should by no means restrict the scope of this invention.

[0029] Fig. 4 is an actual circuit diagram of a charge pump according to another preferred embodiment of this invention. As shown in Fig. 4, the charge pump includes P-type metal oxide semiconductor (PMOS) transistors 402, 404, 406 and 408, N-type metal oxide semiconductor (NMOS) transistors 412, 414, 416 and 418 and capacitors 430 and 440. In addition, the charge pump receives an input voltage V_{IN} from a voltage source (not shown) and a clocking signal CK and an inverted signal CK' from a signal source (not shown).

[0030] One capacitor terminal (or the first terminal of the first capacitor) of the capacitor 430 (or the first capacitor) receives the clocking signal CK. The other capacitor terminal (or the second terminal of the first capacitor) of the capacitor 430 connects with an output terminal V_{OUT1} for outputting the first output voltage. One capacitor terminal (or the first capacitor terminal of the second capacitor) receives the inverted clocking signal CK'. The other capacitor terminal (or the second capacitor terminal of the second capacitor) of the capacitor 440 (or the second capacitor) connects with another output terminal V_{OUT2} for outputting the second output voltage.

[0031] One source/drain terminal (or the first source/drain terminal of the first PMOS transistor) of the PMOS transistor 402 (or the first PMOS transistor) is electrically connected to the capacitor 430 and the substrate (or the substrate of the first PMOS transistor) of the PMOS transistor 402. The other source/drain terminal (or the second source/drain terminal of the first PMOS transistor) of the PMOS transistor 402 is electrically connected to a voltage source for receiving an input voltage V_{IN}. Similarly, one source/drain terminal (or the first source/drain terminal of the second PMOS

transistor) of the PMOS transistor 404 (or the second PMOS transistor) is electrically connected to the capacitor 430 and the substrate (or the substrate of the second PMOS transistor) of the PMOS transistor 404. The other source/drain terminal (or the second source/drain terminal of the second PMOS transistor) of the PMOS transistor 404 is electrically connected to the gate (or the gate of the first PMOS transistor) or the PMOS transistor 402. Furthermore, the gate (or the gate of the second PMOS transistor) of the PMOS transistor 404 is electrically connected to the voltage source for receiving the input voltage V_{IN}.

[0032] One source/drain terminal (or the first source/drain terminal of the third PMOS transistor) of the PMOS transistor 406 (or the third PMOS transistor) is electrically connected to the capacitor 440 and the substrate (or the substrate of the third PMOS transistor) of the PMOS transistor 406. The other source/drain terminal (or the second source/drain terminal of the third PMOS transistor) of the PMOS transistor 406 is electrically connected to the voltage source for receiving an input voltage V_{IN}. Similarly, one source/drain terminal (or the first source/drain terminal of the fourth PMOS transistor) of the PMOS transistor 408 (or the fourth PMOS transistor) is electrically connected to the capacitor 430 and the substrate (or the substrate of the fourth PMOS transistor) of the PMOS transistor 408. The other source/drain terminal (or the second source/drain terminal of the fourth PMOS transistor) of the PMOS transistor 408 is electrically connected to gate (or the gate of the third PMOS transistor) of the PMOS transistor 406. Furthermore, the gate (or the gate of the fourth transistor) of the PMOS transistor 408 is electrically connected to the voltage source for receiving the input voltage V_{IN}.

[0033] The gate (or the gate of the first NMOS transistor) of the NMOS transistor 412 (or the first NMOS transistor) is electrically connected to the voltage source for

receiving the input voltage V_{IN}. One source/drain terminal (or the second source/drain terminal of the first NMOS transistor) of the NMOS transistor 412 is electrically connected to the gate of the PMOS transistor 402. The substrate (or the substrate of the first NMOS transistor) is connected to a ground. One source/drain terminal (or the first source/drain terminal of the second NMOS transistor) of the NMOS transistor 414 (or the second NMOS transistor) and the substrate (or the substrate of the second NMOS transistor) of the NMOS transistor 414 are connected to a ground. The other source/drain terminal (or the second source/drain terminal of the second NMOS transistor) of the NMOS transistor 414 is electrically connected to a source/drain terminal (or the first source/drain terminal of the first NMOS transistor) of the NMOS transistor 412. The gate (or the gate of the second NMOS transistor) of the NMOS transistor 414 receives the inverted clocking signal CK'. The gate (or the gate of the third NMOS transistor) of the NMOS transistor 416 (or the third NMOS transistor) is electrically connected to the voltage source for receiving the input voltage V_{IN}. A source/drain terminal (or the second source/drain terminal of the third NMOS transistor) of the NMOS transistor 416 is electrically connected to the gate of the PMOS transistor 406. The substrate (or the substrate of the third NMOS transistor) of the NMOS transistor 416 is electrically connected to a ground. A source/drain terminal (or the first source/drain terminal of the fourth NMOS transistor) of the NMOS transistor 418 (or the fourth NMOS transistor) and the substrate (the substrate of the fourth NMOS transistor) of the NMOS transistor 418 are electrically connected to a ground. The other source/drain terminal (or the second source/drain terminal of the fourth NMOS transistor) of the NMOS transistor 418 is electrically connected to the source/drain terminal (or the first source/drain terminal of the third NMOS transistor) of the NMOS transistor 416. Furthermore, the gate (or the

gate of the fourth NMOS transistor) of the NMOS transistor 418 receives the clocking signal CK.

[0034] To explain the operation of the charge pump according to this invention, assume the first and the second output voltage is at 0V initially. In addition, assume the fluctuation range of the clocking signal CK and the inverted clocking signal CK' is between 0 to V_{IN} volts and that the initial voltage value of the clocking signal CK is 0 and the initial voltage value of the inverted clocking signal CK' is at V_{IN}.

[0035] At the very beginning, because the voltage value of the inverted clocking signal CK' is at V_{IN}, the NMOS transistor 414 conducts and hence the source/drain terminal of the NMOS transistor 414 and the source/drain terminal of the NMOS transistor 412 are at 0V. Since the gate terminal of the NMOS transistor 412 receives the input voltage V_{IN}, the NMOS transistor 412 conducts and hence the source/drain terminal of the NMOS transistor 412, the source/drain terminal of the PMOS transistor 404 and the gate terminal of the PMOS transistor 402 are at 0V. Because the gate terminal of the PMOS transistor 404 is at V_{IN} while the source/drain is at 0V, the PMOS transistor 404 is non-conductive. On the contrary, because the source/drain terminal of the PMOS transistor 402 receives the input voltage V_{IN} while the gate is at 0V, the PMOS transistor 402 conducts and hence the input voltage starts to charge up the capacitor 430. Since the clocking signal CK is at a 0V, voltage difference between the terminals of the capacitor 430 approaches V_{IN} if sufficient time is given. In other words, the first output voltage from the output terminal V_{OUT1} approaches the input voltage V_{IN}.

[0036] Conversely, because the clocking signal CK is at 0V, the NMOS transistor 418 is non-conductive. Since the gate terminal of the NMOS transistor 416 receives the input voltage V_{IN}, the NMOS transistor 416 conducts and hence the voltage value at the

source/drain terminal of the NMOS transistor 416, the source/drain terminal of the PMOS transistor 406 and the gate of the PMOS transistor 406 approach V_{IN}. Since the voltage value at the gate terminal of the PMOS transistor 408 is V_{IN}, the PMOS transistor 408 is non-conductive. Similarly, because the input voltage V_{IN} received by the source/drain terminal of the PMOS transistor 406 is close to the voltage received by the gate terminal, the PMOS transistor 402 is non-conductive. Therefore, the second output voltage from the output terminal V_{OUT2} is roughly identical to the inverted clocking signal CK'. In other words, the second output voltage from the output terminal V_{OUT2} approaches V_{IN}.

[0037] When the clocking signal CK reverses, that is, the voltage value of the clocking signal CK becomes V_{IN} while the voltage value of the inverted clocking signal CK' becomes 0, both the PMOS transistor 402 and the PMOS transistor 404 are non-conductive according to the aforementioned derivation at the output terminal V_{OUT2}. Hence, due to the transient maintenance of existing voltage differential between the terminals of the capacitor 430, the first output voltage at the output terminal V_{OUT1} is pushed up to $V_{IN} + V_{IN}$, that is, $2*V_{IN}$, transiently. Furthermore, because both the PMOS transistors 402 and 404 are non-conductive, the $2*V_{IN}$ voltage at the output terminal V_{OUT1} can be maintained. On the other hand, when the voltage value of the inverted clocking signal CK' is 0, voltage differential between the two terminals of the capacitor 440 is maintained transiently. Hence, voltage at the capacitor terminal will drop to 0V simultaneously. However, because the PMOS transistors 406 and 408 will conduct, the input voltage V_{IN} will continue to charge up the output terminal V_{OUT2} until the voltage at the output terminal V_{OUT2} almost reaches V_{IN} if sufficient time is allowed.

[0038] Thereafter, as the clocking signal CK reverses, the PMOS transistor 402 and 404 will be conductive again. Thus, voltage at the output terminal V_{OUT1} is

maintained at V_{IN}. On the other hand, because the PMOS transistors 406 and 408 are non-conductive, voltage at the output terminal V_{OUT2} is maintained at V_{IN}. Under the condition that the capacitor terminal 440b receives a voltage V_{IN} from the inverted clocking signal CK', the second output voltage from the output terminal V_{OUT2} is $2*V_{IN}$.

[0039] Henceforth, the first output voltage and the second output voltage from the output terminals V_{OUT1} and V_{OUT2} will fluctuate cyclically between V_{IN} and $2*V_{IN}$. Yet, the gate-substrate interface inside the PMOS transistors 402, 404, 406 and 408 only has to withstand a voltage differential of V_{IN} instead of a voltage differential of $2*V_{IN}$ in a conventional circuit.

[0040] Fig. 5 is an actual circuit diagram of a voltage doubler according to another preferred embodiment of this invention. As shown in Fig. 5, the charge pump 52 is structurally similar to the one in Fig. 4 and hence detailed description of its operation is not repeated here. The charge pump 52 has output terminals similar to the first output terminal V_{OUT1} and the second output terminal V_{OUT2} as shown in Fig. 4, and numbered in Fig. 5 as 550 and 552, respectively. In the same way, when the voltage of the clocking signal and the inverted clocking signal oscillates between $0 \sim V_{IN}$, voltage at the first output terminal V_{OUT1} and the second output terminal V_{OUT2} oscillates at a voltage between $V_{IN} \sim 2*V_{IN}$. In the following, operation of the circuit outside the charge pump 52 is explained in detail.

[0041] Aside from the charge pump 52, the circuit in Fig. 5 further includes four PMOS transistors 562, 564, 566 and 568, a substrate capacitor 570 and an output capacitor 580. One source/drain terminal (or the first source/drain terminal of the fifth PMOS transistor) of the PMOS transistor 562 (or the fifth PMOS transistor) is electrically connected to the aforementioned second output terminal V_{OUT2} of the charge pump 52.

The other source/drain terminal (or the second source/drain terminal of the fifth PMOS transistor) of the PMOS transistor 562 is electrically connected to the substrate (or the substrate of the fifth PMOS transistor) of the PMOS transistor 562. The gate (or the gate of the fifth PMOS transistor) of the PMOS transistor 562 is electrically connected to the aforementioned first output voltage terminal V_{OUT1} of the charge pump 52. One source/drain terminal (or the first source/drain terminal of the sixth PMOS transistor) of the PMOS transistor 564 (or the sixth PMOS transistor) is electrically connected to the first output terminal V_{OUT1}. The other source/drain terminal (or the second source/drain terminal of the sixth PMOS transistor) of the PMOS transistor 564 is electrically connected to the substrate (or the substrate of the sixth PMOS transistor) of the PMOS transistor 564. The gate (or the gate of the sixth PMOS transistor) of the PMOS transistor 564 is electrically connected to the second output terminal V_{OUT2}.

[0042] In addition, one source/drain terminal (or the first source/drain terminal of the seventh PMOS transistor) of the PMOS transistor 566 (or the seventh PMOS transistor) is electrically connected to the second output terminal V_{OUT2}. The other source/drain terminal (or the second source/drain terminal of the seventh PMOS transistor) of the PMOS transistor 566 is electrically connected to a final output terminal 590 for outputting a final output voltage V_0. The substrate (or the substrate of the seventh PMOS transistor) of the PMOS transistor 566 is electrically connected to the substrate and source/drain terminal of the PMOS transistor 562. The gate (or the gate of the seventh PMOS transistor) of the PMOS transistor 566 is electrically connected to the second output voltage terminal V_{OUT2}. One source/drain terminal (or the first source/drain terminal of the eighth PMOS transistor) of the PMOS transistor 568 (or the eighth PMOS transistor) is electrically connected to the first output voltage terminal V_{OUT1}. The other

source/drain terminal (or the second source/drain terminal of the eighth PMOS transistor) of the PMOS transistor 586 is electrically connected to the final output terminal 590. The substrate (or the substrate of the eighth PMOS transistor) of the PMOS transistor 568 is electrically connected to the substrate of the PMOS transistor 564. The gate (or the gate of the eighth PMOS transistor) of the PMOS transistor 568 is electrically connected to the first output voltage terminal V_{OUT1}.

[0043] Finally, one end of the substrate capacitor 570 is electrically connected to a ground while the other end of the substrate capacitor 570 is electrically connected to the substrates of the PMOS transistors 562, 564, 566 and 568. One end of the output capacitor 580 is electrically connected to a ground while the other end is electrically connected to the output terminal 590.

[0044] Assume the first output voltage V_{OUT1} is at V_{IN} and the second output voltage V_{OUT2} is at $2*V_{IN}$ after oscillation in the first output voltage V_{OUT1} and the second output voltage V_{OUT2} is stabilized. Under these conditions, the PMOS transistors 562 and 566 are conductive while the PMOS transistors 564 and 568 are non-conductive so that the second output voltage V_{OUT2} (at a voltage $2*V_{IN}$) charges up the output capacitor 580. When the second output voltage V_{OUT2} becomes V_{IN}, the PMOS transistors 562 and 566 are non-conductive while the PMOS transistor 564 and 568 are conductive so that the first output voltage V_{OUT1} (at a voltage $2*V_{IN}$) charges up the output capacitor 580. Accordingly, if sufficient waiting time is allowed, the final output voltage V_0 at the output terminal 590 will stabilize at a value double that of the input voltage, that is, $2*V_{IN}$.

[0045] Although MOS transistors are used in the circuit of this invention, similar devices such as metal-oxide-semiconductor field effect transistor (MOSFET), enhanced

metal-oxide-semiconductor field effect transistor (enhanced MOSFET) or complementary metal-oxide-semiconductor (CMOS) are also applicable.

[0046] In summary, the voltage difference at the gate-substrate, gate-drain and gate-source interface inside the charge pump of this invention is smaller than the conventional circuit. In particular, peak voltage difference between the gate-substrate is only half the value in the conventional circuit. Consequently, a low pressure CMOS fabrication process can be used to fabricate MOS devices having a voltage push-up capacity identical to the conventional technique but with a longer working life.

[0047] It will be apparent to those skilled in the art that various modifications and variations can be made to the structure of the present invention without departing from the scope or spirit of the invention. In view of the foregoing, it is intended that the present invention cover modifications and variations of this invention provided they fall within the scope of the following claims and their equivalents.